

Syllabus

I. Course Description:

Prerequisites: COP 3223

Corequisites: COT 3100 or MHF 3302 or MAD 2104

Logic design, computer arithmetic, Instruction Set Architecture (MIPS, SPIM simulator), performance, datapath, control unit, memory hierarchy, I/O interface.

II. Recommended Course Textbook:

Computer Organization and Design: The Hardware/Software Interface, Fifth Edition

by David A. Patterson and John L. Hennessy

ISBN: [978-0124077263](https://www.amazon.com/Computer-Organization-Design-5th/dp/0124077263).

III. Basis for Final Grade

Assessment	Percent of Final Grade
Homework	30%
Project	15%
Midterm	25%
Final Exam – 10:00 am, August 6	30%
	100%

Grading Scale (%)

90 – 100	A
80 – 89	B
70 – 79	C
60 – 69	D
0 – 59	F

IV. Assessments

Homework assignments will be assigned throughout the semester. These will be announced in class and posted on the webcourse with their respective due date and time. All items must be submitted on the webcourse by the noted date and time – late work is accepted only at the discretion of the instructor.

The course project will be assigned towards the end of the semester. This is a roughly three-week assignment that can be completed individually or in pairs. More information will be provided on the webcourse. All projects must be turned in on the webcourse no later than the last day of classes.

V. Course Policies

Contact:

Students are welcome to use email or webcourses to contact the instructor or teaching assistants, but understand that responses will not be immediate. To ensure that the email is read as promptly as possible include your Course Number and last name in the subject line. Allow 48 hours for a response, not including weekends.

Webcourses:

Webcourses will be used extensively in this course and students are responsible for checking the webcourse periodically for assignment due dates, assessment offerings, and course announcements. It is recommended that you check the webcourse before each class meeting.

Attendance:

Attendance is not required, but is strongly encouraged. If a student misses a class for any reason, they are expected to review the appropriate material from the course text.

Written Materials:

Non-digital components of the course will be returned to students after grading. If you do not collect these materials, they will be stored at most two semesters.

Academic Dishonesty:

Academic dishonesty in any form will not be tolerated. If you are uncertain as to what constitutes academic dishonesty, please consult The Golden Rule, the University of Central Florida's Student Handbook (<http://www.goldenrule.sdes.ucf.edu/>) for further details. As in all University courses, The Golden Rule Rules of Conduct will be applied. Violations of these rules will result in a record of the infraction being placed in your file and receiving a zero on the work in question AT A MINIMUM.

VI. Course Outcomes

After completing this course, students should:

- Be familiar with various elements of logic design, including Boolean algebra, truth tables, logic gates, Karnaugh maps, latches, and flip-flops
- Be familiar with various data representations in computing systems including binary, hexadecimal, signed/unsigned integers, and floating point numbers
- Be capable of performing arithmetic operations as implemented in computer systems for both integer and floating point numbers
- Be capable of understanding, writing, and debugging simple MIPS assembly programs.
- Be capable of designing and/or expanding a single-cycle data path and its control unit.
- Be familiar with basic concepts of memory hierarchy.
- Understand the performance trade-offs for ISA and cache, and the cost-effectiveness.
- Understand the overall organization and design of computers from programmer's and architect's point of view.
- Be capable of simulating a simple processor using a high-level language such as C.

VII. Course Topics

- Combinational Logic
- Sequential Logic
- Arithmetic Hardware
- Computer Arithmetic
- Instruction Set Architecture
- Datapath and Control Unit
- Pipelining
- Performance
- Memory Hierarchy
- I/O Interface